



Atty Docket No.: RBS2.P031

PATENT

IN THE UNITED STATES PATENT OFFICE

2187
41
RECEIVED

AUG 01 2005

In Re Patent Application of:

First Named Inventor: Garrett, Jr., Billy

Application No.: 09/837,307

Filed: 4/17/2001

Title: MECHANISM FOR ENABLING FULL DATA BUS
UTILIZATION WITHOUT INCREASING DATA
GRANULARITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiner: Dinh, Ngoc V.

Technology Center 2100

Art Unit: 2187

I hereby certify that this correspondence is being deposited
with the United States Postal Service as first class mail
with sufficient postage in an envelope addressed to the
Commissioner for Patents, P.O. Box 1450, Alexandria VA
22313-1450 on July 25, 2005
Kyle S. Okada
(Name of Person Mailing Correspondence)

Kyle S. Okada
Signature

July 25, 2005
Date

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

Sir:

Enclosed is an Information Disclosure Citation Form 1449/PTO together with a copy of each reference cited therein, excluding U.S. Patents and Published U.S. Patent Applications. It is respectfully requested that the cited references be considered and that the enclosed copy of the Form 1449/PTO be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant.

This Information Disclosure Statement is being submitted pursuant to 37 CFR 1.97(b). No fee is believed to be due.

Pursuant to 37 CFR 1.97(h), the submission of this Information Disclosure Statement is not to be construed as an admission that the information cited in this statement is material to patentability.

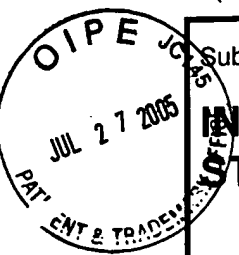
The Commissioner is hereby authorized to charge any fees which may be required in connection with this submission to Deposit Account No. 501914.

Respectfully submitted,

SHEMWELL GREGORY & COURTNEY LLP

Date July 25, 2005

Charles E. Shemwell, Reg. No. 40,171
Tel. 408-236-6645



Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Page 1 of 4

Application No.	09/837,307
Filed	4/17/2001
First Inventor	Garrett, Jr., Billy
Art Unit	2187
Examiner	Dinh, Ngoc V.
Atty. Docket No.	RBS2.P031

U.S. Patent Documents					
Examiner Initials*	US Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication	Relevant Pages, Columns, Lines
	Number	Kind			
	2001/0037428	A1	Hsu et al.	Nov., 2001	
	2003/0052885	A1	Hampel et al.	Mar., 2003	
	20040019756	A1	Perego et al.	1/29/2004	
	4670745		O'Malley et al.	Jun., 1987	
	4766538		Miyoshi	8/23/1988	
	4768157		Chauvel et al.	Aug., 1988	
	4837465		Rubinstein	Jun., 1989	
	4985867		Ishii et al.	1/15/1991	
	5146592		Pfeiffer et al.	Sep., 1992	
	5394528		Kobayashi et al.	2/28/1995	
	5530814		Wong et al.	6/25/1996	
	5546346		Agata et al.	Aug., 1996	
	5559970		Sharma	9/24/1996	
	5614855		Lee et al.	3/25/1997	
	5652870		Yamasaki et al.	7/29/1997	
	5655113		Leung et al.	8/5/1997	
	5717871		Hsieh et al.	2/10/1998	
	5717901		Sung et al.	2/10/1998	
	5748561		Hotta	May., 1998	
	5751657		Hotta	May., 1998	
	5787267		Leung et al.	7/28/1998	
	5793998		Copeland et al.	8/11/1998	
	5801985		Roohparvar et al.	9/1/1998	
	5852725		Yen	12/22/1998	

RECEIVED

AUG 01 2005

Technology Center 2100

Examiner Signature		Date Considered	
-------------------------------	--	----------------------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.



Substitute for Form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Page 2 of 4

Application No.	09/837,307
Filed	4/17/2001
First Inventor	Garrett, Jr., Billy
Art Unit	2187
Examiner	Dinh, Ngoc V.
Atty. Docket No.	RBS2.P031

U.S. Patent Documents

Examiner Initials*	US Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication	Relevant Pages, Columns, Lines
	Number	Kind			
	5893927		Hovis	4/13/1999	
	5936885		Morita et al.	Aug., 1999	
	5958033		Schubert et al.	9/28/1999	
	6034878		Osaka et al.	3/7/2000	
	6047347		Hansen et al.	4/4/2000	
	6125157		Donnelly et al.	9/26/2000	
	6138185		Nelson et al.	10/24/2000	
	6141273		Ku et al.	10/31/2000	
	6144220		Young	11/7/2000	
	6247084		Apostol et al.	Jun., 2001	
	6311313		Camporese et al.	10/30/2001	
	6366995		Vilkov et al.	Apr., 2002	
	6393543		Vilkov et al.	May., 2002	
	6625687		Halbert et al.	9/23/2003	
	6754120		Bellows et al.	Jun., 2004	
	6825841		Hampel et al.	Nov., 2004	
	RE37409		Barth et al.	Oct., 2001	

RECEIVED**AUG 01 2005**

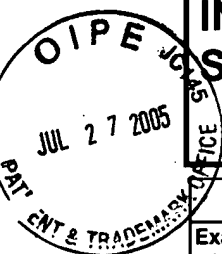
Technology Center 2100

Foreign Patent Documents

Examiner Initials*	Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication	Relevant Pages, Columns, Lines	Trans- lation
	Number	Kind				
	EP0887737	B1		1/22/2003		
	GB2367400	A		4/3/2002		

Examiner Signature		Date Considered	
-------------------------------	--	----------------------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.



Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Page 3 of 4	Application No.	09/837,307
	Filed	4/17/2001
	First Inventor	Garrett, Jr., Billy
	Art Unit	2187
	Examiner	Dinh, Ngoc V.
	Atty. Docket No.	RBS2.P031

Non Patent Literature Documents

Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans- lation
	C. Yoo et al., "A 1.8V 700 Mb/s/pin 512Mb DDR-II SDRAM with On-Die Termination and Off-Chip Driver Calibration, IEEE International Solid-State Circuits Conference ISSCC 2003/Session 17/SRAM and DRAM/ Paper 17.7, pp. 312-313 and 496, plus Visuals Supplement on pp. 250-251 and 535	
	Fairchild Semiconductor, "Design Optimization Techniques for Double Data Rate SDRAM Modules," Jul. 2000. 6 pages.	
	IEEE 100, "The Authoritative Dictionary of IEEE Standards Terms", Seventh Edition. Critical piece first to Cross bar switch (page 252).	
	Kirihata et al., "A 390-mm ² , 16-Bank, 1-Gb DDR SDRAM with Hybrid Bitline Architecture", IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999; pages 1580-1588	
	Masumoto, "Configurable On-Chip RAM Incorporated Into High Speed Logic Array", Proceedings of the IEEE 1985 Custom Integrated Circuits Conference, May 20-23, 1985; pages 240-243.	
	Micron Technology, Inc., "Graphics DDR3 DRAM MT44H8M32- 2 Meg x 32 x 4 Banks," Advance Data Sheet, Copyright 2003, pp. 1-67	
	Micron Technology, Inc., "Micron Synchronous DRAM 128Mb:x32 SDRAM," pp. 1-52, Rev. 9/00.	
	Minutes of Meeting No. 70, JC-42.3 Committee on RAM Memories, March 9, 1994, Orlando, Florida, 72 pages (see, in particular, page 62).	
	NVIDIA Corporation, "GeForce3: Lightspeed Memory Architecture," NVIDIA Corporation Technical Brief, pp. 1-9, date unknown.	

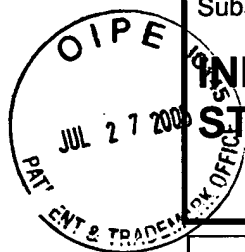
RECEIVED

AUG 01 2005

Technology Center 21

Examiner Signature		Date Considered	
-------------------------------	--	----------------------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.



Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Page 4 of 4	Application No.	09/837,307
	Filed	4/17/2001
	First Inventor	Garrett, Jr., Billy
	Art Unit	2187
	Examiner	Dinh, Ngoc V.
	Atty. Docket No.	RBS2.P031

Non Patent Literature Documents		
Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans- lation
	S. Takase and N.i Kushiya, "WP 24.1 A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE Journal of Solid State Circuits, Vol. 34, No. 11, November 1999, pp. 1600-1606	
	S. Takase and N.i Kushiya, "WP 24.1 A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE International Solid-State Circuits Conference, 4 pages plus ISSCC Slide Supplement pp. 348-349 and 506-507	
	Samsung Electronics, "SDRAM Device Operations," 41 pages, date unknown.	
	Satoh et al., "A 209K-Transistor ECL Gate Array with RAM", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989; pages 1275-1281.	
	Zhao et al., "An 18 Mb, 12.3 GB/s CMOS Pipeline-Burst Cache SRAM with 1.54 Gb/s/pin", IEEE International Solid-State Circuits Conference, 1999; 10 pages.	

00

RECEIVED

AUG 01 2005

Technology Center 2100

Examiner Signature		Date Considered	
-------------------------------	--	----------------------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.